GWORLD

40G-BASE-LR4 10km QSFP+ Optical Transceiver

GTR3QP1L

Features

- ● Hot Pluggable QSFP+ MSA package
- ● IEEE 802.3ba 40GBASE-LR4 compliant
- ● SFF-8436 and IEC61754-20 compliant
- ● Up to 10km for G.652 SMF
- ● Receiver: 4 x 10Gb/s PIN ROSA
- ● Transmitter: uncooled 4 x 10Gb/s CWDM TOSA (1271,1291,1311,1331nm)
- ● 4x10G Electrical Serial Interface (XLPPI)
- ● 2-wire serial interface with Digital Diagnostic
- ● +3.3V power supply
- ● Power consumption less than 2.5W
- ● Compact size: 72.4 x 18.35 x 8.5 mm
- ● Operating case temperature: 0 to +70 ℃
- ● Duplex LC Receptacle
- ● ROHs-6 compliant

Applications

- ● 40GBase-LR4 40G Ethernet

Description

GWorld Opto's GTR3QP1L QSFP+ transceivers are designed for use in 40 Gigabit Ethernet links over 10km single module fiber, and it compliant to the QSFP+ MSA and IEEE 802.3ba 40GBASE-LR4. Digital diagnostics are available via 2-wire serial interface as specified in the QSFP+ MSA.

The transceiver's designs are optimized for high performance and cost efficiency to provide customers the best solutions for Datacom and Telecom applications.

The transceiver is RoHS-6 compliant and lead-free per Directive 2002/95/EC.

Product Selection

GTR3QP1L

G: GWorld
TR: Transceiver
QP1:   QSFP+ Solution 1
L: 10km

1 40Gb/s QSFP+ electrical parameters

1.1 Absolute Maximum Ratings

The limit of the maximum value is shown as below Table 1. (If operating out the limit of the maximum value will cause permanent damage).

Table 1 40Gb/s QSFP+ module limit the maximum value

Parameter	Symbol	Conditions	Min.	Max	Unit
Storage temperature（case）	T_{stg}	—	-40	+85	℃
Relative humidity	RH	0	—	85	%
Damage Threshold for Receiver	Pmax	—	—	+10.0	dBm
Power Supply	Vcc 3.3V	—	-0.5	+4.0	V
	Vcc 5.0V	—	—	—	V
Input LVTTL and LVCMOS signal level	Vio	—	-0.5	+3.6	V
Input amplitude on TxDATA[1:4] P/N	Vtxdata_diff	Differential AC coupled	—	1.6	Vpp
ESD Sensitivity on module and all host pins	HBM	Human Body model R=1.5K, C=100pF	—	2000	V

1.2 Recommended operating conditions

The recommended working conditions are shown as below Table 2.

Table 2 40Gb/s QSFP+ recommended working conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	Tc	0	—	+70	℃
Operating wavelength	λ	1264.5	—	1337.5	nm
Supply voltage	Vcc 3.3V	+3.14	+3.3	+3.47	V
Supply Current	Icc 3.3V	—	—	710	mA
Power dissipation	P	—	—	2.5	W
Link Distance	L	—	—	10km	G.652 SMF

2 40Gb/s QSFP+ Specifications

2.1 Optical Specifications

Table 3 40Gb/s QSFP+ Optical Specifications (transmission distance 10km)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmitter						
Channel data rate				10.3125		Gbps
Aggregate data rate				41.25		Gbps
Data rate variation			-100		+100	ppm
Lane Center Wavelength	λc_{T0}			1264.5 – 1277.5		nm

	λc_{T1}			1284.5 – 1297.5		
	λc_{T2}			1304.5 – 1317.5		
	λc_{T3}			1324.5 – 1337.5		
Total Average Launch Power	Pout		—	—	8.3	dBm
Average Launch Power per Lane[1]	Peach		-7	—	2.3	dBm
Optical Modulation Amplitude[2]	OMA		-4	—	3.5	dBm
Difference in Launch power between any two lances(OMA)			—	—	6.5	dB
Launch power in OMA minus TDP	Pomatdp		-4.8	—	—	dBm
Average Launch Power of TX_DIS Transmitter per lane	Poff	TX_DIS=H	—	—	-30	dBm
Optical Eye Mask			Compliant to IEEE 802.3 Clause 40Gbase-LR4			
Extinction Ratio	E_R		3.5	—	—	dB
Dispersion Penalty	DP	10km SMF	—	—	2.3	dB
Relative Intensity Noise	RIN	Mod off	—	—	-128	dB/Hz
Transmitter reflectance[3]	Tef		—	—	-12	dB
Receiver						
Channel data rate				10.3125		Gbps
Data rate variation			-100		+100	ppm
Lane Center Wavelength	λc_{T0}			1264.5 – 1277.5		nm
	λc_{T1}			1284.5 – 1297.5		
	λc_{T2}			1304.5 – 1317.5		
	λc_{T3}			1324.5 – 1337.5		
Receiver Overload[4]	Pov		3.3	—	—	dBm
Average receiver power[5]	Rpow		-13.7	—	2.3	dBm
Receiver power OMA	Rovl		—	—	3.5	dBm
Difference in receive power between any two lanes(OMA)			—	—	7.5	dB
Receiver Sensitivity per lane[6]	Psen		—	—	-11.5	dBm
Stressed Receiver Sensitivity[7]	Psen_str		—	—	-9.9	dBm
Receiver Reflectance	Ref		—	—	-12	dB
Conditions of stressed receiver sensitivity test						
Vertical eye closure penalty[8]			—	—	1.6	dB
Stressed eye jitter			—	—	0.3	UI

Note1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note2. Even if the TDP < 0.8dB, the OMA (min) must exceed this value.

Note3. Transmitter reflectance is defined for the transmitter.

Note4. The receiver shall be able to tolerate, without damage, continuous exposure

to an optical input signal with this average power level.

Note5. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note6. Receiver sensitivity (OMA), each lane (max) is informative.

Note7. Measured with conformance test signal for BER = $10E^{-12}$.

Note8. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

2.2 Electrical specifications

Table 4 40Gb/s QSFP+ Electrical Interface Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmitter						
Differential Data Input Amplitude	Vin-diff		120	—	800	mVpp
Input Differential Impedance	Zdiff		80	100	120	ohm
AC common mode input voltage tolerance(RMS)			15			mV
Differential to common-mode input return loss			10			dB[1]
J2 Jitter Tolerance			0.17			UI
J9 Jitter Tolerance			0.29			UI
Receiver						
Differential Data Output amplitude	Vout-diff		320	—	800	mVpp
Output Differential Impedance	Zdiff		80	100	120	ohm
AC common-mode output voltage(RMS)					7.5	mV
Differential output return loss		IEEE 802.3ba-2010	See 86A.4.2.1			dB[1]
Common-mode output return loss		IEEE 802.3ba-2010	See 86A.4.2.2			dB[1]
J2 Jitter Tolerance					0.42	UI
J9 Jitter Tolerance					0.65	UI
Output transition time	Tr	20%~80%	28	—	—	ps

Notes1. 10 MHz to 11.1 GHz

3 40Gb/s QSFP+ Function Diagram

3.1 Internal reference structure

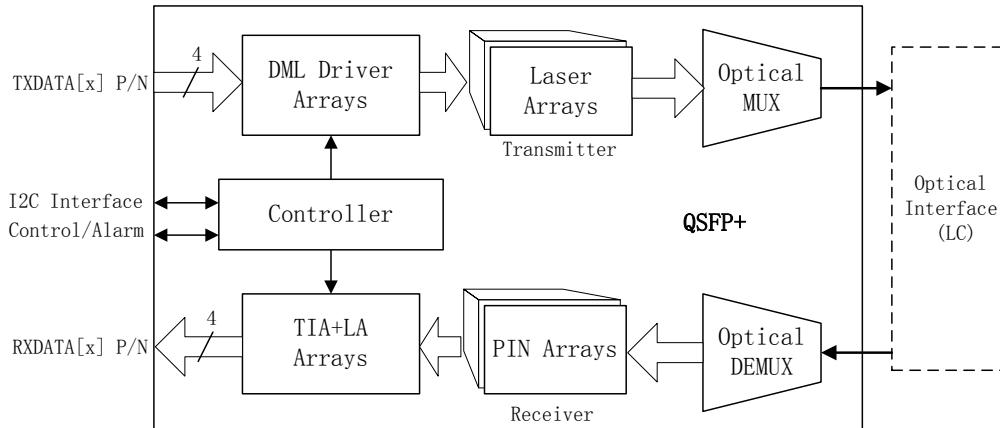The internal structure of 40Gb/s QSFP+ shown as Figure 1.

Figure 1. 10km 40Gb/s QSFP+ internal structure

3.2 Recommended Interface Circuit
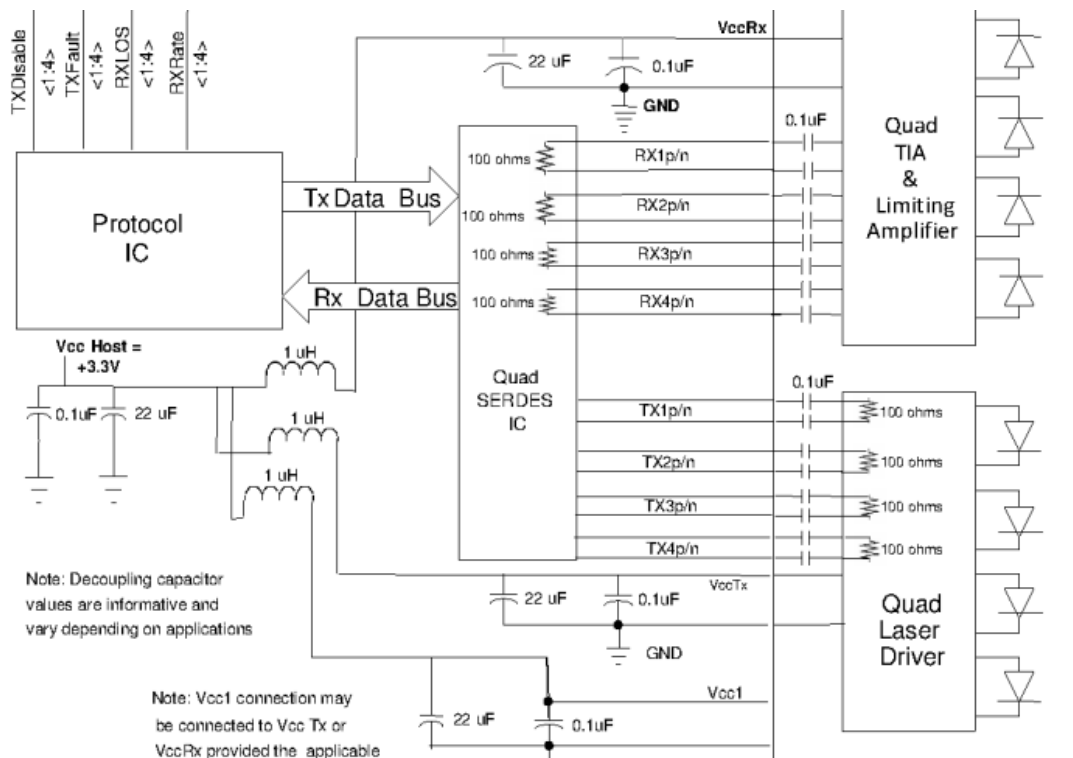

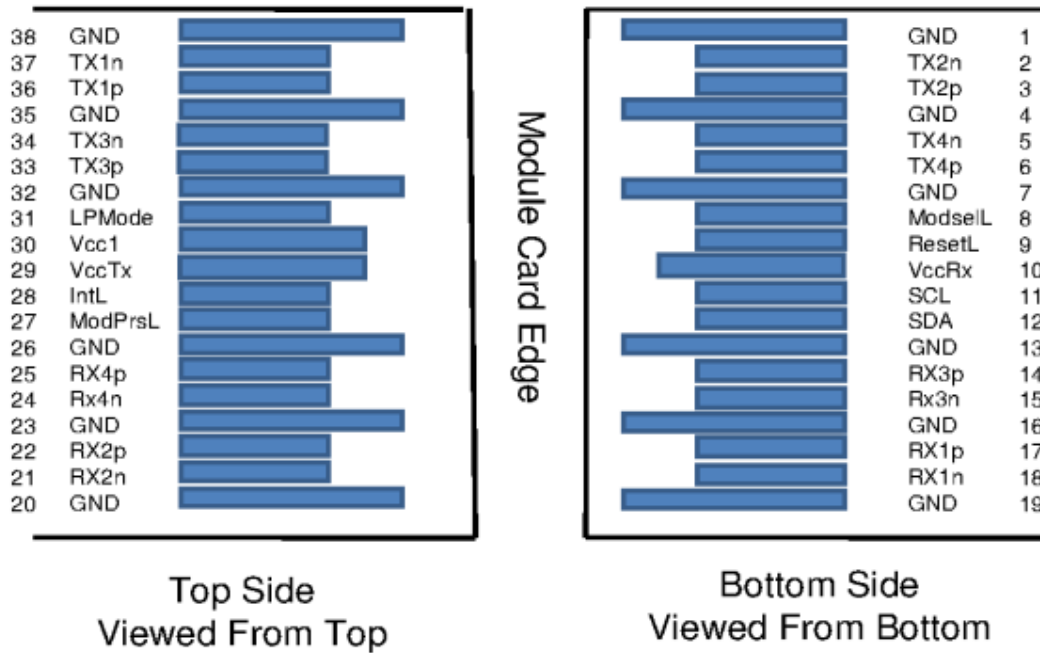
Figure 2. Recommended Interface Circuit

3.3 Pin layout

Figure 3. QSFP+ Module Pad Layout

3.4 Pin definition

Table 5 40Gb/s QSFP+ Pin Definition(first raw)

PIN	Name	Logic	Description
1	GND		Ground
2	Tx2n	CML-I	Transmitter Invert Data Input
3	Tx2p	CML-I	Transmitter Non-Invert Data Input
4	GND		Ground
5	Tx4n	CML-I	Transmitter Invert Data Input
6	Tx4p	CML-I	Transmitter Non-Invert Data Input
7	GND		Ground
8	ModSelL	LVTTL-I	Module Select
9	ResetL	LVTTL-I	Module Reset
10	Vcc Rx		+3.3V Power Supply Receiver
11	SCL	LVCMOS-I/O	2-wire serial interface clock
12	SDA	LVCMOS-I/O	2-wire serial interface data
13	GND		Ground
14	Rx3p	CML-O	Receiver Non-Invert Data Output
15	Rx3n	CML-O	Receiver Invert Data Output
16	GND		Ground
17	Rx1p	CML-O	Receiver Non-Invert Data Output
18	Rx1n	CML-O	Receiver Invert Data Output
19	GND		Ground

Table 6 40Gb/s QSFP+ Pin Definition(second raw)

PIN	Name	Logic	Description
20	GND		Ground
21	Rx2n	CML-O	Receiver Invert Data Output
22	Rx2p	CML-O	Receiver Non-Invert Data Output
23	GND		Ground
24	Rx4n	CML-O	Receiver Invert Data Output
25	Rx4p	CML-O	Receiver Non-Invert Data Output
26	GND		Ground
27	ModPrsL	LVTTL-O	Module Present
28	IntL	LVTTL-O	Interrupt
29	Vcc Tx		+3.3V Power supply transmitter
30	Vcc1		+3.3V Power supply
31	LPMode	LVTTL-O	Low Power Mode
32	GND		Ground
33	Tx3p	CML-I	Transmitter Non-Invert Data Input
34	Tx3n	CML-I	Transmitter Invert Data Input
35	GND		Ground
36	Tx1p	CML-I	Transmitter Non-Invert Data Input
37	Tx1n	CML-I	Transmitter Invert Data Input
38	GND		Ground

Note1: GND is the symbol for signal and supply (power) common for the QSFP+ module. Connect these directly to the host board signal-common ground plane.

Note2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Patch of QSFP+ pin is 0.8mm, width of QSFP+ pin is 0.35mm and maximum current of QSFP+ pin is 0.5A.

The host board power supply should be well filtered shown in Figure 4, to meet the noise filtering requirements in most system and achieve QSFP+ module specifications performance.
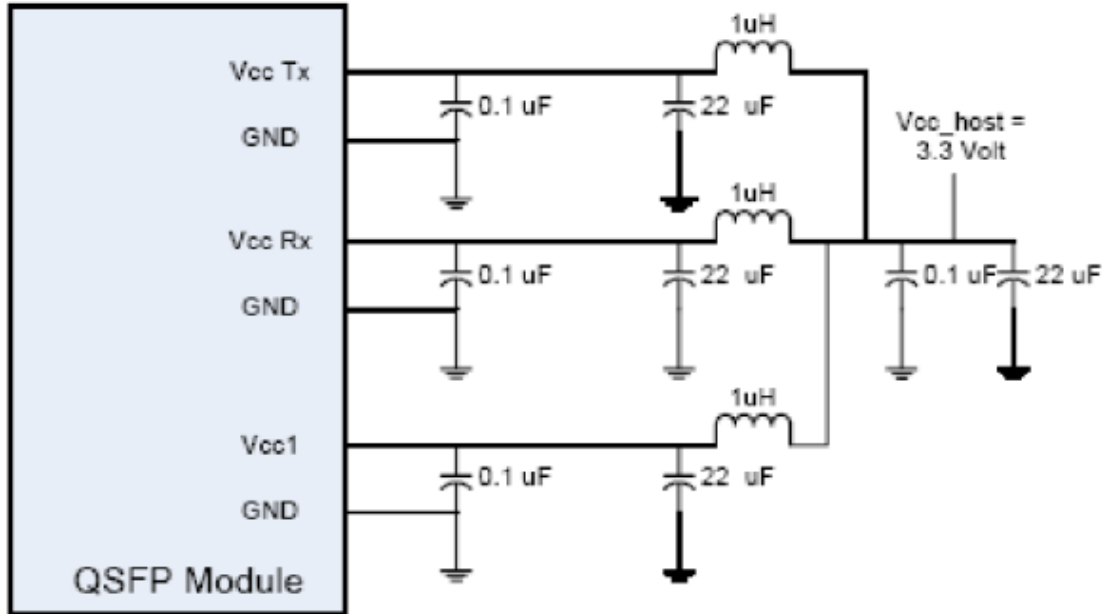
Figure 4. Example of Host Board Supply Filtering Network

4 40Gb/s QSFP+ Mechanical Specifications

40Gb/s QSFP+ mechanical dimensions should be compliant with SFF-8436. Detailed dimensions are shown in Figure 5.
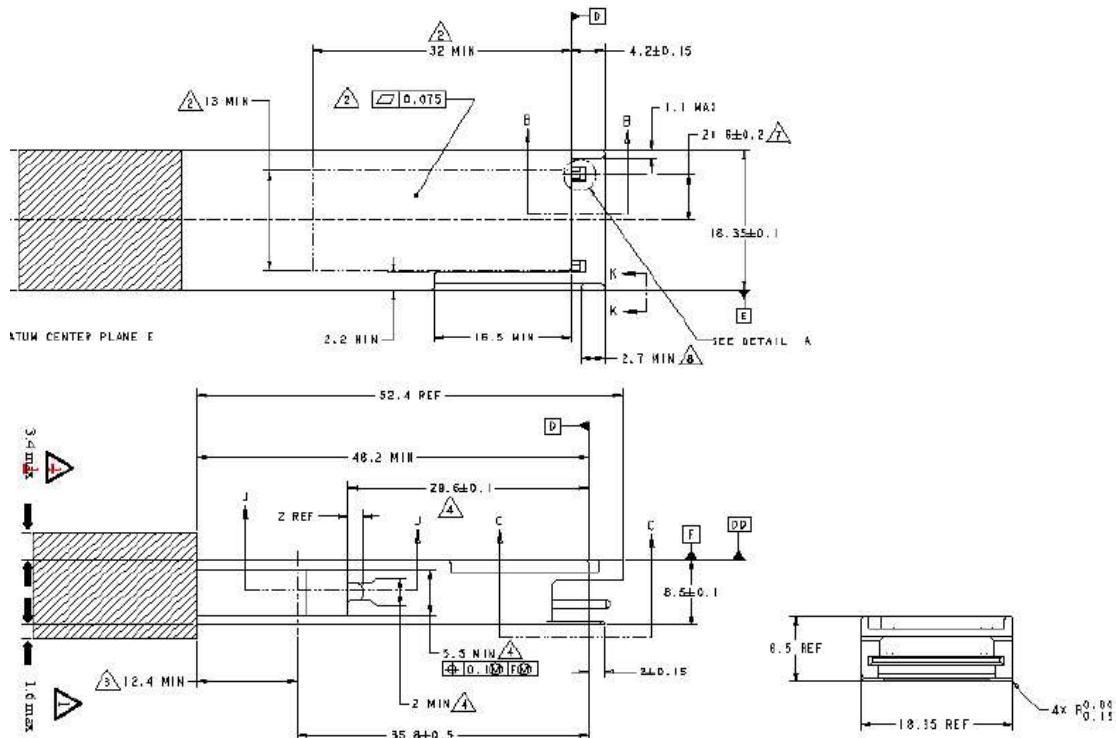

Figure 5. 40Gb/s QSFP+ Mechanical Dimensions

The mechanical dimensions of the electrical connectors on the QSFP+ module PCB are shown in Figure 6.
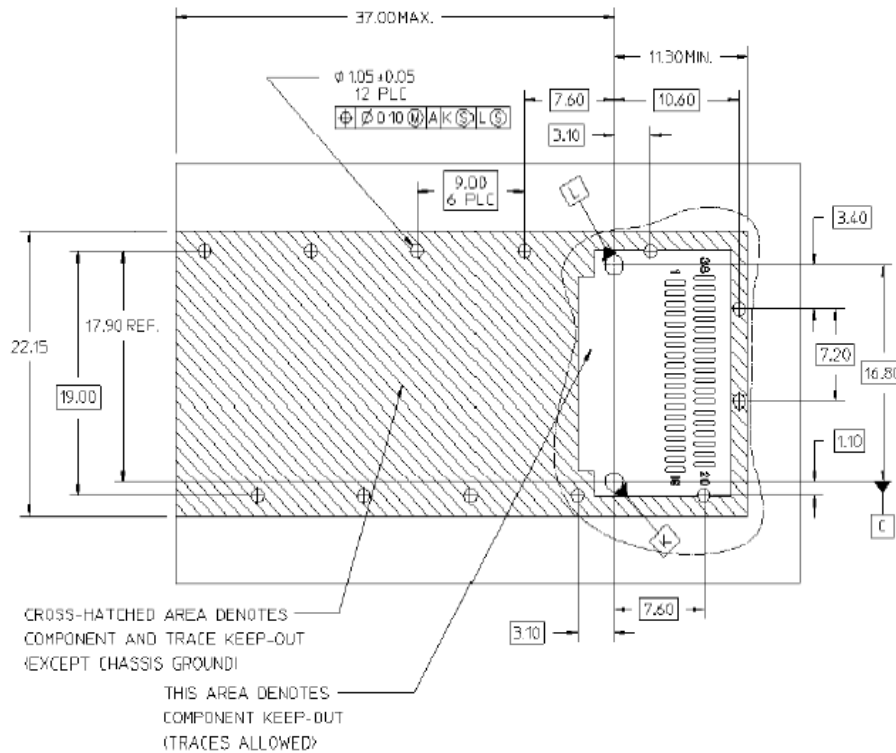
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Figure 6   Mechanical Dimensions of Electrical Connectors on QSFP+ module PCB

Table 7 specifies the fiber and fiber connector for 40Gb/s QSFP+, for applications, a configuration of the optical connector should be supported.

Table 7   Fiber Connector Type

Parameter	Specification	Units
Weight	<250	g
Flatness	<0.05	mm
Roughness	<6.5	Ra
Connector	Straight/Angled LC/PC	

5 Management Interface

GWorld GTR3QP1L QSFP+ transceivers support the 2-wire serial communication protocol as defined in the SFF-8436 MSA. It is very closely related to the E^2PROM defined in the GBIC standard, with the same electrical specifications.

A management interface, as already commonly used in other form factors like GBIC, SFP, and XFP, is specified in order to enable flexible use of the module by the user. The specification has been changed in order to adopt the use of a multi-channel module. Some timing requirements are critical especially for a multi-channel device, so the interface speed has been increased. This QSFP+ specification is based on the INF8438 specification however it is not backward compatible. Address 128 Page00 is used to indicate the use of the QSFP+ memory map rather than the QSFP memory map.

The standard QSFP+ serial ID provides access to identification information that describes the transceiver's capabilities, standard interfaces, manufacturer, and other information.

Additionally, GWorld QSFP+ transceivers provide a enhanced digital diagnostic monitoring interface, which allows real-time access to device operating parameters such as transceiver temperature, laser bias current, transmitted optical power, received optical power and transceiver supply voltage. It also defines a sophisticated system of alarm and warning flags, which alerts end-users when particular operating parameters are outside of a factory set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller inside the transceiver, which is accessed through a 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL, Mod Def 1) is generated by the host. The positive edge clocks data into the QSFP+ transceiver into those segments of the E^2PROM that are not write-protected. The negative edge clocks data from the QSFP+ transceiver. The serial data signal (SDA, Mod Def 2) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

6　Ordering Information

Table 8　Order Information

Part No.	Application	Data Rate	Transmitter	Receiver	Fiber Type	Connector
GTR3QP1L	40GBase-LR4 40G Ethernet	41.2Gb/s	4*10G CWDM TOSA	4*10G PIN ROSA	SMF	LC/PC

7　Revision History

Rev.	Date	Modification	Note
V1.0	Jun 30th, 2013		New

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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